Amendments to the Specification:

Please replace the paragraph beginning at page 3, line 20, with the following rewritten paragraph:

Multiple register contexts are obtained in the ManArray processor by controlling how the array S/P-bit in the ManArray instruction format is used in conjunction with a context ~~switch~~ select bit (CSB) for the context selection of the PE register file or the SP register file. In arrays consisting of more than a single PE, the software controllable context switch mechanism is used to reconfigure the array to take advantage of the multiple context support the merged SP/PE provides. For example, a 1x1 can be configured as a 1x1 with context-0 and as a 1x0 with context-1, a 1x2 can be configured as a 1x2 with context-0 and as a 1x1 with context-1, and a 1x5 can be configured as a 1x5 with context-0 and as a 2x2 with context-1. Other array configurations are clearly possible using the present invention. In the 1x5/2x2 case, the two contexts could be a 1x5 with the sequential control context in the SP register files with context-0 and a 2x2 array context, where the sequential control context uses the PE0's register files with context-1.

Please replace the paragraph beginning at page 5, line 2, with the following rewritten paragraph:

Further details of a presently preferred ManArray core, architecture, and instructions for use in conjunction with the present invention are found in U.S. Patent Application Serial No. 08/885,310 filed June 30, 1997, now U.S. Patent No. 6,023,753, U.S. Patent Application Serial No. 08/949,122 filed October 10, 1997, now U.S. Patent No. 6,167,502, U.S. Patent Application

Serial No. 09/169,255 filed October 9, 1998, now U.S. Patent No. 6,343,356, U.S. Patent Application Serial No. 09/169,256 filed October 9, 1998, now U.S. Patent No. 6,167,501, U.S. Patent Application Serial No. 09/169,072 filed October 9, 1998, now U.S. Patent No. 6,219,776, U.S. Patent Application Serial No. 09/187,539 filed November 6, 1998, now U.S. Patent No. 6,151,668, U.S. Patent Application Serial No. 09/205,~~558~~ 588 filed December 4, 1998, now U.S. Patent No. 6,173,389, U.S. Patent Application Serial No. 09/215,081 filed December 18, 1998, now U.S. Patent No. 6,101,592, U.S. Patent Application Serial No. 09/228,374 filed January 12, 1999, now U.S. Patent No. 6,216,223, ~~and entitled "Methods and Apparatus to Dynamically Reconfigure the Instruction Pipeline of an Indirect Very Long Instruction Word Scalable Processor",~~ U.S. Patent Application Serial No. 09/238,446 filed January 28, 1999, now U.S. Patent No. 6,366,999, U.S. Patent Application Serial No. 09/267,570 filed March 12, 1999, now U.S. Patent No. 6,446,190, U.S. Patent Application Serial No. 09/337,839 filed June 22, 1999, U.S. Patent Application Serial No. 09/350,191 filed July 9, 1999, now U.S. Patent No. 6,356,994, U.S. Patent Application Serial No. 09/422,015 filed October 21, 1999, now U.S. Patent No. 6,408,382, ~~entitled "Methods and Apparatus for Abbreviated Instruction and Configurable Processor Architecture",~~ U.S. Patent Application Serial No. 09/432,705 filed November 2, 1999, now U.S. Patent No. 6,697,427, ~~entitled "Methods and Apparatus for Improved Motion Estimation for Video Encoding",~~ U.S. Patent Application Serial No. 09/471,217 filed December 23, 1999, now U.S. Patent No. 6,260,082, ~~entitled "Methods and Apparatus for Providing Data Transfer Control",~~ U.S. Patent Application Serial No. 09/472,372 filed December 23, 1999, now U.S. Patent No. 6,256,683, ~~entitled "Methods and Apparatus for~~

~~Providing Direct Memory Access Control",~~ U.S. Patent Application Serial No. 09/596,103 ~~entitled "Methods and Apparatus for Data Dependent Address Operations and Efficient Variable Length Code Decoding in a VLIW Processor"~~ filed June 16, 2000, now U.S. Patent No. 6,397,324, U.S. Patent Application Serial No. 09/598,566 ~~entitled "Methods and Apparatus for Generalized Event Detection and Action Specification in a Processor"~~ filed June 21, 2000, now U.S. Patent No. 6,735,690, U.S. Patent Application Serial No. 09/598,564 ~~entitled "Methods and Apparatus for Initiating and Resynchronizing Multi-Cycle SIMD Instructions"~~ filed June 21, 2000, now U.S. Patent No. 6,622,234, ~~U.S. Patent Application Serial No. 09/598,558 entitled "Methods and Apparatus for Providing Manifold Array (ManArray) Program Context Switch with Array Reconfiguration Control" filed June 21, 2000,~~ and U.S. Patent Application Serial No. 09/598,084 ~~entitled "Methods and Apparatus for Establishing Port Priority Functions in a VLIW Processor"~~ filed June 21, 2000, now U.S. Patent No. 6,654,870, as well as, Provisional Application Serial No. 60/113,637 entitled "Methods and Apparatus for Providing Direct Memory Access (DMA) Engine" filed December 23, 1998, Provisional Application Serial No. 60/113,555 entitled "Methods and Apparatus Providing Transfer Control" filed December 23, 1998, Provisional Application Serial No. 60/139,946 entitled "Methods and Apparatus for Data Dependent Address Operations and Efficient Variable Length Code Decoding in a VLIW Processor" filed June 18, 1999, Provisional Application Serial No. 60/140,245 entitled "Methods and Apparatus for Generalized Event Detection and Action Specification in a Processor" filed June 21, 1999, Provisional Application Serial No. 60/140,163 entitled "Methods and Apparatus for Improved Efficiency in Pipeline Simulation and Emulation" filed June 21, 1999, Provisional

Application Serial No. 60/140,162 entitled "Methods and Apparatus for Initiating and Re-Synchronizing Multi-Cycle SIMD Instructions" filed June 21, 1999, Provisional Application Serial No. 60/140,244 entitled "Methods and Apparatus for Providing One-By-One Manifold Array (1x1 ManArray) Program Context Control" filed June 21, 1999, Provisional Application Serial No. 60/140,325 entitled "Methods and Apparatus for Establishing Port Priority Function in a VLIW Processor" filed June 21, 1999, Provisional Application Serial No. 60/140,425 entitled "Methods and Apparatus for Parallel Processing Utilizing a Manifold Array (ManArray) Architecture and Instruction Syntax" filed June 22, 1999, Provisional Application Serial No. 60/165,337 entitled "Efficient Cosine Transform Implementations on the ManArray Architecture" filed November 12, 1999, and Provisional Application Serial No. 60/171,911 entitled "Methods and Apparatus for DMA Loading of Very Long Instruction Word Memory" filed December 23, 1999, Provisional Application Serial No. 60/184,668 entitled "Methods and Apparatus for Providing Bit-Reversal and Multicast Functions Utilizing DMA Controller" filed February 24, 2000, Provisional Application Serial No. 60/184,529 entitled "Methods and Apparatus for Scalable Array Processor Interrupt Detection and Response" filed February 24, 2000, Provisional Application Serial No. 60/184,560 entitled "Methods and Apparatus for Flexible Strength Coprocessing Interface" filed February 24, 2000, and Provisional Application Serial No. 60/203,629 entitled "Methods and Apparatus for Power Control in a Scalable Array of Processor Elements" filed May 12, 2000, respectively, all of which are assigned to the assignee of the present invention and incorporated by reference herein in their entirety.

Please replace the paragraph beginning at page 9, line 18, with the following rewritten paragraph:

To provide for efficient context switching within a ManArray processor, a processor mode bit is provided in a control register such as a processor state register in a miscellaneous register file (MRF) shown, for example, in data memory interface controller 125. This bit is identified as a context ~~switch~~ select bit (CSB). Fig. 2 illustrates a functional view of a system 200 for implementing the present invention. An S/P-bit and CSB bit control logic unit 202 contains the CSB and override logic. The control logic unit 202 provides enable signals 204 and 206 to multiplexers 208 and 210, respectively, to select where the result data from the execution units 212 are to be written. The result data is selectively written either to the SP configurable register file 214 or to the PE configurable register file 216. The control logic unit 202 also provides a select signal 218 to a multiplexer 220 to control which block of registers 214 or 216 that execution units 212 read data from. It is noted that in Fig. 2, the execution units 212 in the ManArray iVLIW processor may advantageously comprise five heterogeneous execution units which correspond to the five execution units 131 in Fig. 1. Also, the buses, multiplexers, and select control signals shown in Fig. 2 are indicated with multiple line since in the ManArray processor such as shown in Fig. 1 there are eight 32-bit read ports and four 32-bit write ports for each 16x32-bit portion of both the reconfigurable register files and each requires separate selection and control depending upon the instruction in execution and the machine state.

Please replace the paragraph beginning at page 10, line 11, with the following rewritten paragraph:

Specifically, the CSB bit in conjunction with the S/P-bit in PE0's control logic allows efficient context switching between tasks. Control specification 300 of Fig. 3 lists three exemplary array configurations and describes the register file use and array operating configuration for SP or PE instructions, as specified by the instruction's S/P-bit, also referred to as the SP/PE selection bit, depending upon the setting of the CSB bit. Table 310 indicates the ManArray architecture definition of the S/P-bit, which is present in the execution units' instruction formats. In general, other register files including the reconfigurable compute register files are shared between contexts. Specifically, in Fig. 3, the register files that are indicated to be shared are the address register file (ARF), the compute register file (CRF), and selected MRF and special purpose registers (SPRs) used by the execution units. The physical MxN column 304 indicates the physical array organization of PEs in the core processor, while the operating MxN column 312 depends upon the CSB value. It is noted that with the CSB bit set to zero, as seen in control specification entries 320, 322, 330, 332, 340, and 342, the SP operates in context-0 with SP instructions only executing in the SP on SP resources and PE instructions only executing in any or all of the PEs on PE resources. With the CSB bit set to a one, as seen in control specification entries 324, 326, 334, 336, 344, and 346, the SP operates in context-1 which uses the PE0's register files. As described by this invention, each MxN core is a two context processor where one of the contexts uses SP-only resources for sequential control while the other context uses PE0's resources for sequential control.

Please replace the paragraph beginning at page 12, line 9, with the following rewritten paragraph:

This approach may also be used on larger arrays, such as 1x5 ManArray processor 500 shown in Fig. 5 having four additional PEs 551, 553, 555, and 557 in addition to PE0 which is part of SP/PE0 501. Fig. 5 uses the following notation for the PEs: PE virtual ID/physical ID. In processor 500 of Fig. 5, there are five physical PEs which operate as a 1x5 with the SP using the SP register files 511 as context-0 when the CSB bit is inactive. When the CSB bit is active, the PE array reconfigures itself into a 2x2 with the SP taking over PE0's register files 527, and other inferred files, for context-1. Each of the PEs switches to a virtual identity such that code written for a 2x2 PE array functions correctly on the reconfigured organization. Each PE supports the decode function for the two identified PEs. For example, PE 2/3 555 responds as PE3, its physical ID, when the CSB bit is inactive and responds as PE2, its virtual ID, when the CSB bit is active. The concepts of virtual PEs and cluster switch control is covered in further detail in U.S. ~~Application Serial No. 09/169,256~~ Patent No. 6,167,501 entitled "Methods and Apparatus for ManArray PE-PE Switch Control". Note that the cluster switch is extended to support five PEs in Fig. 5 which is allowed by the general form of the ManArray interconnection network and covered in additional detail in U.S. Patent No. 6,023,753 entitled "Manifold Array Processor" and U.S. ~~Application Serial No. 08/949,122~~ Patent No. 6,167,502 entitled "Methods and Apparatus for Manifold Array Processing", both of which are incorporated herein by reference in their entirety.

Please replace the paragraph beginning at page 13, line 7, with the following rewritten paragraph:

To further support the context switch mechanism and provide support for multiple contexts, an additional mechanism is added to allow one of the register files to be saved and restored from memory in the background while a task is using another register file referred to as the foreground register file. One mechanism used for this takes advantage of unused load and store unit instruction slots to perform this context switch save and restore operation. Essentially, "background" store and load instructions, together with a means of indexing through a register file, are activated whenever a task is not executing a foreground load or store instruction. A pair of background address registers is required to provide the store and load addresses for the register context switch. The "background" store and load instructions are pre-stored context switch save and restore instructions which, when enabled, operate in the background until the save and restore operation has completed. Use of the eventpoint architecture is one mechanism that can be set up to test for the lack of foreground store and load instruction execution and trigger a background store and load instruction to execute. Suitable eventpoint architecture is covered in more detail in U.S. Provisional Application Serial No. 60/140,245 entitled "Methods and Apparatus for Generalized Event Detection and Action Specification in a Processor" and U.S. ~~Application Serial No. _____ having the same title and filed June 21, 2000~~ Patent Application Serial No. 09/598,566, filed June 21, 2000, now U.S. Patent No. 6,735,690, both of which are incorporated by reference herein in their entirety. A status bit is also used to indicate the progress of the context switch so that, if preempted, it could be allowed to complete before another program context was initiated. Further details of a presently preferred register file indexing mechanism are provided in U.S. Patent Application Serial No. 09/267,570 entitled

"Register File Indexing Methods and Apparatus for Providing Indirect Control of Register Addressing in a VLIW Processor" filed March 12, 1999, now U.S. Patent No. 6,446,190, and incorporated by reference herein in its entirety. This register file indexing mechanism is preferably used for register file access.